EXHIBIT C

Paper No. __

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

Case No. IPR2021-00155
Patent No. 10,416,961

PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq

that saved power by reducing precision in its floating-point operations to whatever precision was needed for a particular application. Dockser, [0003]-[0007]; Goodin, ¶ 35.

The challenged claims encompass this prior-art concept. Claim 1 recites a device comprising an LPHDR execution unit adapted to execute an operation on an input signal representing a first numerical value to produce an output signal representing a second numerical value, and a generic computing device adapted to control operation of the execution unit. Nothing more. The remainder of the claim simply characterizes the execution unit's performance by reciting its minimum dynamic range and degree of imprecision. Goodin, ¶¶ 36, 38.

II. SUMMARY OF GROUNDS

The challenged claims would have been obvious under § 103 as the following grounds demonstrate. Each reference below (none of which was before the examiner) is prior art under pre-AIA § 102(b) even assuming the challenged claims were entitled to their earliest claimed priority date (they are not as Petitioner's concurrently filed petition demonstrates).

Ground Number and Reference(s)		Claims
1	Dockser (Ex. 1007)	1-2, 4-5, 10, 13-14
2	Dockser, Tong (Ex. 1008)	1-2, 4-5, 10, 13-14, 21, 24-25
3	Dockser, MacMillan (Ex. 1009)	1-5, 10, 13-14
4	Dockser, Tong, MacMillan	1-5, 10, 13-14, 21, 23-25

Ground 1: Dockser discloses a "floating-point processor" (FPP) that performs "multiplication" at a selectable "precision." Dockser, Abstract, [0012]. Dockser's FPP is an HDR execution unit whose standard floating-point inputs exceed the claimed minimum dynamic range. *Infra* § V.B.3. Recognizing that some applications do not require full-precision operations, Dockser's FPP operates at a selectable reduced precision to conserve power in applications where greater precision is unnecessary. A selected "subprecision" is achieved by removing power to any desired number of least-significant mantissa bits, dropping those bits (resulting in less precision) and reducing power consumption. Dockser, [0014]; Goodin, ¶¶ 291-292. Dockser discloses an example that drops all but the 9 most-significant bits, resulting in imprecision meeting the claimed minimum error amounts. *Infra* § V.B.4. Dockser renders obvious claims 1-2, 4-5, 10, and 13-14.

Ground 2: Tong teaches reducing the number of mantissa bits to conserve power, and discloses experimental results demonstrating the optimum balance of precision and power consumption is achieved using just 5 mantissa bits for certain applications. *Infra* § VI.A. The Dockser/Tong combination, in which Tong's optimized precision levels are used in Dockser's LPHDR execution unit, renders obvious the same claims rendered obvious by Ground 1, and meets the claimed minimum error amounts by even greater margins. Tong teaches to emulate in

software a device comprising an LPHDR execution unit; thus Dockser/Tong also meets claims 21 and 24-25.

Ground 3: MacMillan discloses a computer system with multiple floating-point execution units operating in parallel. *Infra* § VII.A. Based on MacMillan, a POSA would have been motivated to implement a device with multiple Dockser FPPs operating in parallel. The resulting device (Dockser/MacMillan) meets dependent claim 3's requirement of multiple LPHDR execution units, and provides an alternative basis for meeting the "plurality of components" in independent claim 10. MacMillan's "CPU" that controls the execution units (MacMillan, 10:27-53, 13:12-13, 13:38-62) provides an alternative basis for meeting claim 1's "computing device adapted to control the… execution unit" and claim 2's "CPU." *Infra* §§ VII.B-VII.E.

Ground 4: It would have been obvious to implement the Dockser/MacMillan device with the FPPs operating at Tong's precision levels. This Dockser/Tong/MacMillan combination meets the same claims met collectively by Grounds 2 and 3, and also dependent claim 23 which recites a parallel architecture (taught by MacMillan) and emulating the LPHDR execution units in software (taught by Tong).